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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,880	12/19/2001	John Guzek	42390P13271	1290

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EXAMINER
TRAN, LONG K

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,880	GUZEK ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) 16-20 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-15, drawn to a device, classified in class 257, subclass 678.

II. Claims 16-20, drawn to a method of forming the device, classified in class 438, subclass 424.

2. The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as product made and process of making. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the device may be formed by a materially different process such as depositing the dielectric material prior to forming the second conductive region as opposed to forming the clearances.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. During a telephone conversation between Examiner Renzo Rocchegiani and Mr. Paul Mendonfa on February 12, 2003 a provisional election was made without traverse

to prosecute the invention of the product made, claims 1-15. Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 3i' CFR 1.17(i).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1** and **2** are rejected under 35 U.S.C. 102(b) as being anticipated by Patil et al. (US Patent No. 5,672,911).

Regarding claim **1**, figures 5A – 9E illustrate an integrated circuit chip package comprising: a metal substrate core 524 including regions 524a, 524c, 524b and 524d electrically isolated from each other by insulating gap 530a and 530b (col. 9, lines 8+).

Regarding claim **2**, figures 5A – 9E illustrate region (m) of the metal substrate is coupling with an operating voltage of an integrated circuit chip 502.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims **3 – 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Patil et al. (US Patent No. 5,672,911) in view of Ahn et al. (US Patent No. 6,432,724).

Regarding claims **3 – 7**, Patil et al. disclose the claimed invention of claim 1. However, Patil et al. do not explicitly teach at least one of the regions of the substrate core is coupled with digital ground of an integrated circuit; illustrate at least one of the regions of the substrate core is coupled with analog ground of an integrated circuit chip.

It is conventional and also taught by Ahn et al. that multiple chips mounted on the single substrate in a system module typically include different circuits, i.e., some analog circuits and some digital circuits. This requires a low impedance ground 106 (fig. 7) in the system module to suppress digital noise that may appear in the analog circuits of these mixed mode circuits (col. 1, lines 36 – 41)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form metal substrate core in Patil et al.'s integrated circuit chip package with a buried low impedance ground as taught by Ahn et al. in order to suppress digital noise in the analog circuits of a single substrate.

Regarding claims **8 – 11**, figures 5A – 9E illustrate an integrated circuit chip package comprising: a metal substrate core 524 including regions 524a, 524c, 524b

and 524d electrically isolated from each other by insulating gap 530a and 530b (col. 9, lines 8+).

However, Patil et al. do not explicitly teach at least one of the regions of the substrate core is coupled with digital ground of an integrated circuit; illustrate at least one of the regions of the substrate core is coupled with analog ground of an integrated circuit chip.

It is conventional and also taught by Ahn et al. that multiple chips mounted on the single substrate in a system module typically include different circuits, i.e., some analog circuits and some digital circuits. This requires a low impedance ground 106 (fig. 7) in the system module to suppress digital noise that may appear in the analog circuits of these mixed mode circuits (col. 1, lines 36 – 41)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form metal substrate core in Patil et al.'s integrated circuit chip package with a buried low impedance ground as taught by Ahn et al. in order to suppress digital noise in the analog circuits of a single substrate.

Regarding claims **12 – 15**, figures 5A – 9E illustrate an integrated circuit chip package comprising: a metal substrate core 524 including regions 524a, 524c, 524b and 524d electrically isolated from each other by insulating gap 530a and 530b (col. 9, lines 8+); and has input and output signals routed through it (col. 1, lines 35 – 48).

However, Patil et al. do not explicitly teach at least one of the regions of the substrate core is coupled with digital ground of an integrated circuit; illustrate at least

one of the regions of the substrate core is coupled with analog ground of an integrated circuit chip.

It is conventional and also taught by Ahn et al. that multiple chips mounted on the single substrate in a system module typically include different circuits, i.e., some analog circuits and some digital circuits. This requires a low impedance ground 106 (fig. 7) in the system module to suppress digital noise that may appear in the analog circuits of these mixed mode circuits (col. 1, lines 36 – 41)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form metal substrate core in Patil et al.'s integrated circuit chip package with a buried low impedance ground as taught by Ahn et al. in order to suppress digital noise in the analog circuits of a single substrate.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Murata (US Patent Application Publication No. 2002/0030272), Gandhi et al. (US Patent 6,085,415), Hammond et al. (US Patent No. 6,518,502), Gaku et al. (US Patent No. 6,097,089), Sylvester (US Patent No. 6,248,959) and Butt (US Patent No. 5,014,159) discloses an integrated circuit chip package similar to that of Patil et al. (US Patent No. 5,672,911) and Ahn et al. (US Patent No. 6,432,724).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 703-305-5482. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7466 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

LONG TRAN

May 15, 2003

HOAI HO
PRIMARY EXAMINER